Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of patterning a semiconductor region, comprising:
providing a patterned mask above the semiconductor region; and
etching a portion of the semiconductor region exposed by the patterned mask in an environment including a polymerizing fluorocarbon, and at least one non-polymerizing substance selected from the group consisting of non-polymerizing fluorocarbons and hydrogenated fluorocarbons.

[c2] A method as claimed in claim 1, wherein the etching is performed anisotropically.

[c3] A method as claimed in claim 2, wherein the etching is performed in an essentially vertical direction, such that a pattern resulting from the etching has a substantially straight sidewall.

[c4] A method as claimed in claim 1, wherein the environment further includes nitrogen.

[c5] A method as claimed in claim 1, wherein the polymerizing fluorocarbon includes at least one substance selected

from the group consisting of chlorine-free fluorocarbons having a high ratio of carbon to fluorine atoms, and the non-polymerizing fluorocarbon is selected from the group consisting of fluorocarbons having a low ratio of carbon to fluorine atoms, the environment further including nitrogen.

[c6] A method as claimed in claim 5, wherein the environment further includes a plasma.

[c7] A method as claimed in claim 6, wherein the environment has a pressure ranging between about 2 milliTorr and about 100 milliTorr.

[c8] A method as claimed in claim 4, wherein the semiconductor region includes a first semiconductor layer disposed above a second semiconductor layer, the first semiconductor layer being heavily doped, and the second semiconductor layer being no more than lightly doped, wherein portions of the first and second semiconductor layers are patterned by the etching to have substantially straight sidewalls.

[c9] A method as claimed in claim 8, wherein at least portions of the semiconductor region patterned by the etching have at least one form selected from the group consisting of polycrystalline and amorphous.

[c10] A method as claimed in claim 9, wherein the portions patterned by the etching have polycrystalline form.

[c11] A method as claimed in claim 8, wherein the patterned mask includes an anti-reflective coating (ARC).

[c12] A method as claimed in claim 11, wherein the patterned mask includes a hardmask layer disposed below the ARC and above the first semiconductor layer.

[c13] A method as claimed in claim 12, wherein the hardmask layer includes an oxide.

[c14] A method of patterning a semiconductor region, comprising:
providing a patterned mask above the semiconductor region; and
etching a portion of the semiconductor region exposed by the patterned mask in an environment including at least one substance selected from the group consisting of chlorine-free fluorocarbons having a high ratio of carbon to fluorine atoms, and at least one substance selected from the group consisting of: (a) fluorocarbons having a low ratio of ratio of carbon to fluorine atoms, and (b) hydrogenated fluorocarbons.

[c15] A method as claimed in claim 14, wherein the etching is

performed anisotropically.

[c16] A method as claimed in claim 15, wherein the etching is performed in an essentially vertical direction, such that a pattern resulting from the etching has a substantially straight sidewall.

[c17] A method as claimed in claim 16, wherein the environment further includes nitrogen.

[c18] A method as claimed in claim 17, wherein the environment further includes a plasma.

[c19] A method as claimed in claim 18, wherein the environment has a pressure ranging between about 2 milliTorr and about 100 milliTorr.

[c20] A method as claimed in claim 17, wherein the semiconductor region includes a first semiconductor layer disposed above a second semiconductor layer, the first semiconductor layer being heavily doped, and the second semiconductor layer being no more than lightly doped, wherein the etching patterns portions of the first and second semiconductor layers, such that a pattern resulting from the etching has a substantially straight sidewall.

[c21] A method as claimed in claim 20, wherein at least por-

tions of the first and second semiconductor layers have a form selected from the group consisting of polycrystalline and amorphous.

[c22] A method as claimed in claim 21, wherein the portions patterned by the etching have polycrystalline form.

[c23] A method as claimed in claim 22, wherein the patterned mask includes an anti-reflective coating (ARC).

[c24] A method as claimed in claim 23, wherein the patterned mask includes a hardmask layer disposed below the ARC and above the first semiconductor layer.

[c25] A method as claimed in claim 24, wherein the hardmask layer includes an oxide.

[c26] A method of patterning a layered stack including a first essentially polycrystalline semiconductor layer having a first dopant concentration and a second essentially polycrystalline semiconductor layer having a second dopant concentration, the first dopant concentration being greater than about 100 times the second dopant concentration, the method comprising:
providing a patterned mask above the layered stack; and
etching a portion of the first semiconductor layer exposed by the patterned mask; and
etching a portion of the second semiconductor layer un-

derlying the etched portion of the first semiconductor layer, wherein the etching is performed in an environment including nitrogen, at least one substance selected from the group consisting of chlorine-free fluorocarbons having a high ratio of carbon to fluorine atoms, and at least one substance selected from the group consisting of fluorocarbons having a low ratio of ratio of carbon to fluorine atoms, and hydrogenated fluorocarbons.

[c27] A method as claimed in claim 26, wherein the etching is performed in an essentially vertical direction, such that a pattern resulting from the etching has a substantially straight sidewall.

[c28] A method as claimed in claim 27, wherein the patterned mask includes an anti-reflective coating (ARC).

[c29] A method as claimed in claim 28, wherein the patterned mask includes a hardmask layer disposed below the ARC and above the first semiconductor layer.

[c30] A method as claimed in claim 29, wherein the environment further includes a plasma.